

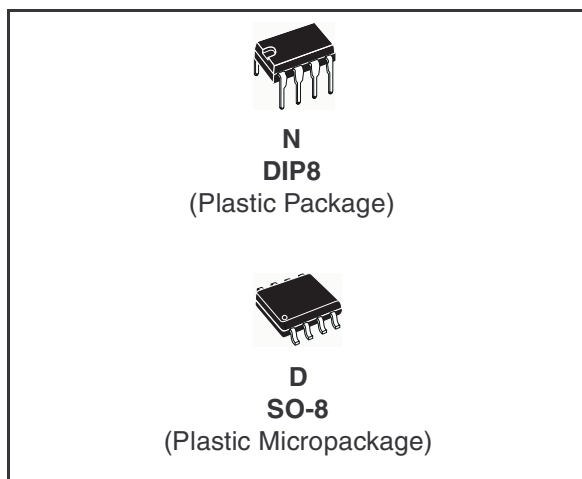
## Precision Dual Operational Amplifier

- Low input offset voltage: 500 $\mu$ V max.
- Low power consumption
- Short circuit protection
- Low distortion, low noise
- High gain-bandwidth product: 3MHz
- High channel separation
- ESD protection 2kV
- Macromodel included in this specification

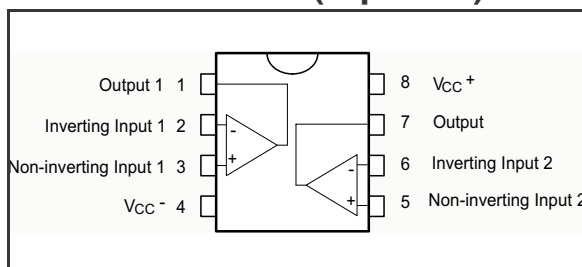
### Description

The TS512 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product.

The circuit presents very stable electrical characteristics over the entire supply voltage range, and is particularly intended for professional and telecom applications (active filter, etc.).



### Pin Connections (top view)



### Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS512IN/AIN	-40, + 125°C	DIP8	Tube	
TS512ID/IDT/AID/AIDT		SO-8	Tube or Tape & Reel	
TS512IYD/IYDT		SO14 (automotive grade level)		512IY
TS512AIYD/AIYDT				512AIY

# 1 Absolute Maximum Ratings

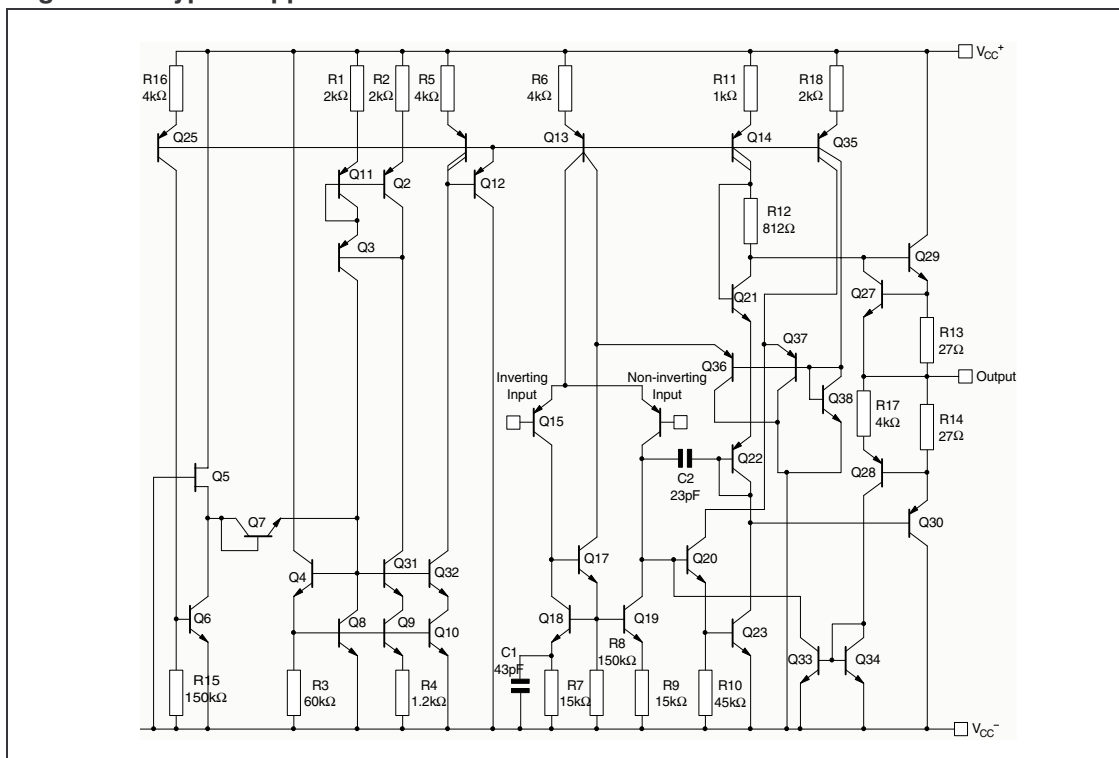
**Table 1. Key parameters and their absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	$\pm 18$	V
$V_i$	Input Voltage	$\pm V_{CC}$	
$V_{id}$	Differential Input Voltage	$\pm(V_{CC} - 1)$	
$T_{oper}$	Operating Free-Air Temperature Range	-40 to +125	°C
$P_{tot}$	Power Dissipation at $T_{amb} = 70^{\circ}\text{C}$ <sup>(1)</sup>	500	mW
$T_j$	Junction Temperature	+ 150	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$V_{CC}$	Supply Voltage	$\pm 18$	V

1. Power dissipation must be considered to ensure maximum junction temperature ( $T_j$ ) is not exceeded.

## 2 Schematic Diagram (1/2 TS512)

Figure 1. Typical application schematic



### 3 ELECTRICAL CHARACTERISTICS

**Table 2.**  $V_{CC} = \pm 15V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current		0.7	1.2	mA
$I_{ib}$	Input Bias Current $T_{min} \leq T_{op} \leq T_{max}$		50	150 300	nA
$R_i$	Input Resistance, $f = 1kHz$		1		M $\Omega$
$V_{io}$	Input Offset Voltage TS512 TS512A $T_{min} \leq T_{op} \leq T_{max}$ TS512 TS512A		0.5	2.5 0.5 3.5 1.5	mV
$\Delta V_{io}$	Input Offset Voltage Drift $T_{min} \leq T_{op} \leq T_{max}$		2		$\mu V/^{\circ}C$
$I_{io}$	Input Offset Current $T_{min} \leq T_{op} \leq T_{max}$		5	20 40	nA
$\Delta I_{io}$	Input Offset Current Drift $T_{min} \leq T_{op} \leq T_{max}$		0.08		$\frac{nA}{^{\circ}C}$
$I_{os}$	Output Short Circuit Current		23		mA
$A_{vd}$	Large Signal Voltage Gain $R_L = 2k\Omega$ , $V_{CC} = \pm 15V$ $V_{CC} = \pm 4V$	90	100 95		dB
GBP	Gain-bandwidth Product, $f = 100kHz$	1.8	3		MHz
$e_n$	Equivalent Input Noise Voltage, $f = 1kHz$ $R_s = 50\Omega$ $R_s = 1k\Omega$ $R_s = 10k\Omega$		8 10 18		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion $A_v = 20dB$ , $R_L = 2k\Omega$ $V_o = 2V_{pp}$ , $f = 1kHz$		0.03		%
$\pm V_{opp}$	Output Voltage Swing $R_L = 2k\Omega$ , $V_{CC} = \pm 15V$ $V_{CC} = \pm 4V$	$\pm 13$	$\pm 3$		V
$V_{opp}$	Large Signal Voltage Swing $R_L = 10k\Omega$ , $f = 10kHz$		28		$V_{pp}$
SR	Slew Rate Unity Gain, $R_L = 2k\Omega$	0.8	1.5		V/ $\mu s$
CMR	Common Mode Rejection Ratio $V_{ic} = \pm 10V$	90			dB
SVR	Supply Voltage Rejection Ratio	90			dB

**Table 2.**  $V_{CC} = \pm 15V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{O1}/V_{O2}$	Channel Separation, $f = 1kHz$		120		dB
$V_{io}$	Input Offset Voltage TS512 TS512A $T_{min} \leq T_{op} \leq T_{max}$ TS512 TS512A		0.5	2.5 0.5 3.5 1.5	mv
$\Delta V_{io}$	Input Offset Voltage Drift $T_{min} \leq T_{op} \leq T_{max}$		2		$\mu V/^{\circ}C$
$I_{io}$	Input Offset Current $T_{min} \leq T_{op} \leq T_{max}$		5	20 40	nA

**Table 3.**  $V_{CC} = \pm 15V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Conditions	Value	Unit
$V_{io}$		0	mV
$A_{vd}$	$R_L = 2k\Omega$	100	V/mV
$I_{cc}$	No load, per operator	350	$\mu A$
$V_{icm}$		-13.5 to 13.5	V
$V_{OH}$	$R_L = 2k\Omega$	+13	V
$V_{OL}$	$R_L = 2k\Omega$	-13	V
$I_{sink}$	$V_o = 0V$	23	mA
$I_{source}$	$V_o = 0V$	23	mA
GBP	$R_L = 2k\Omega$ , $C_L = 100pF$	3	MHz
SR	$R_L = 2k\Omega$	1.4	V/ $\mu s$
$\phi_m$	$R_L = 2k\Omega$ , $C_L = 100pF$	55	Degrees

## 4 Macromodels

**Note:** *Note: Please consider following remarks before using this macromodel:*

*All models are a trade-off between accuracy and complexity (i.e. simulation time).*

*Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.*

*A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its goal is to illustrate the main parameters of the product.*

*Data issued from macromodels used outside of its specified conditions (Vcc, Temperature, etc.) or even worse: outside of the device operating conditions (Vcc, Vicm, etc.) are not reliable in any way.*

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

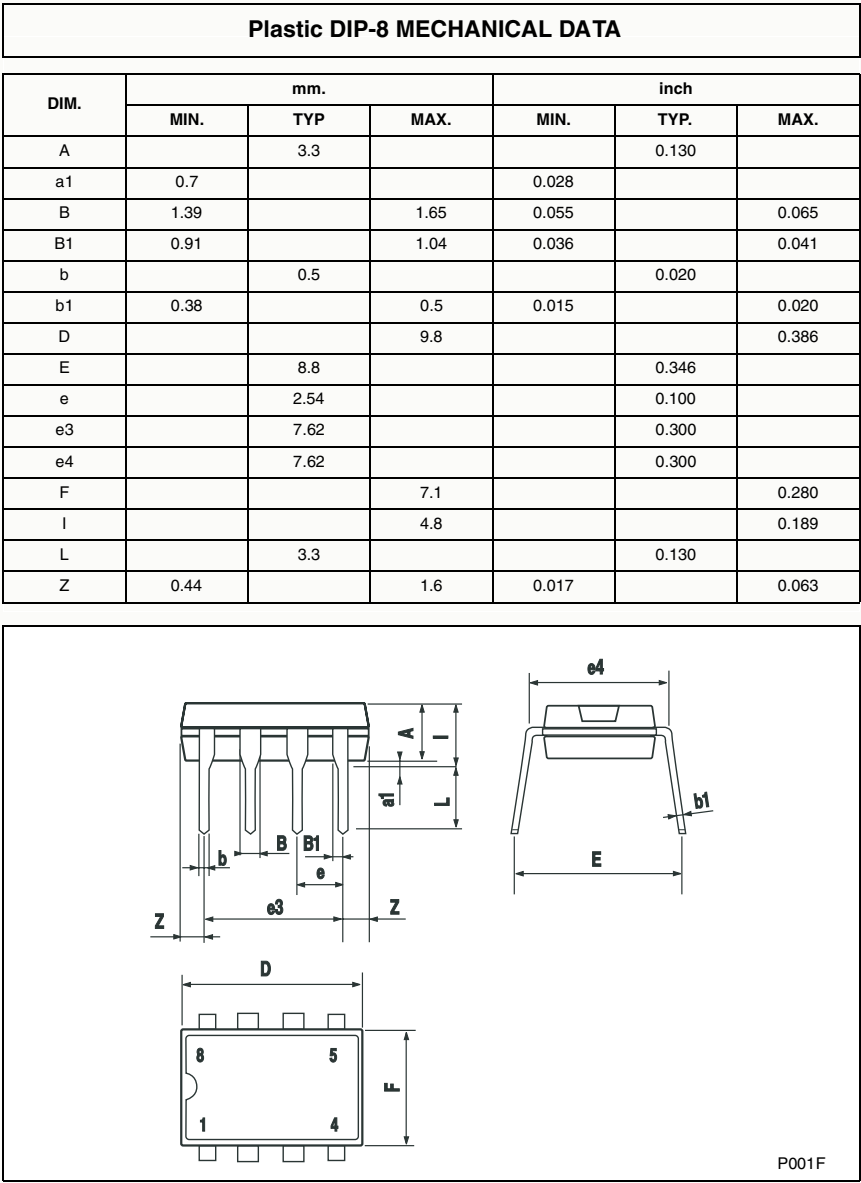
.SUBCKT TS512 1 3 2 4 5 (analog)
*****
.MODEL MDTH D IS=1E-8 KF=6.565195E-17 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 1.061852E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 12.47E-10
DINN 17 13 MDTH 400E-12
VIN 17 5 1.500000E+00
DINR 15 18 MDTH 400E-12
VIP 4 18 1.500000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 1.000000E-02
FIBN 5 1 VOFP 1.000000E-02
* AMPLIFYING STAGE
FIP 5 19 VOFP 9.000000E+02
```

```
FIN 5 19 VOFN 9.000000E+02
RG1 19 5 1.727221E+06
RG2 19 4 1.727221E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 6.521739E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 6.521739E+03
VINM 5 27 1.500000E+02
GCOMP 5 4 4 5 6.485084E-04
RPM1 5 80 1E+06
RPM2 4 80 1E+06
GAVPH 5 82 19 80 2.59E-03
RAVPHGH 82 4 771
RAVPHGB 82 5 771
RAVPHDH 82 83 1000
RAVPHDB 82 84 1000
CAVPHH 4 83 0.331E-09
CAVPHB 5 84 0.331E-09
EOUT 26 23 82 5 1
VOUT 23 5 0
ROUT 26 3 6.498455E+01
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 1.742230E+00
DON 24 19 MDTH 400E-12
VON 24 5 1.742230E+00
.ENDS
```

# 5 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

## 5.1 DIP8 Package

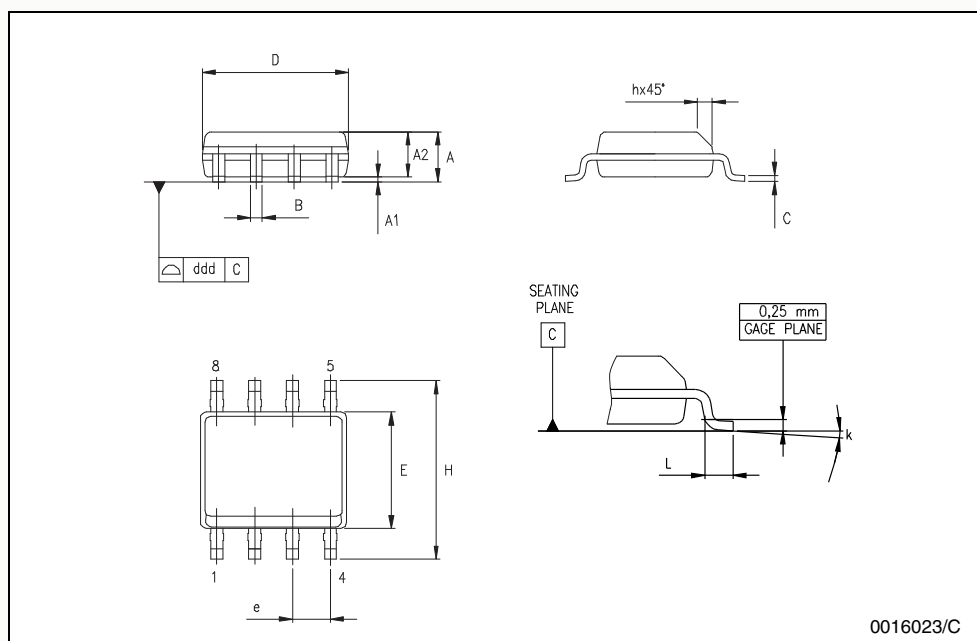




## 5.2 SO-8 Package

**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



## 6 Revision History

Date	Revision	Changes
November 2001	1	Initial release.
June 2005	2	PPAP references inserted in the datasheet see table order code p1

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